What is claimed is:

1. A method for increasing the capacitance of deep trench capacitors, comprising:

providing a substrate;

forming a pad structure on the substrate;

forming a patterned photoresist layer on the pad structure, wherein a trench region is defined by the region uncovered by the patterned photoresist layer;

forming a trench in the substrate using the patterned photoresist layer and the pad structure as an etching mask;

removing the patterned photoresist layer;

forming a trench capacitor in the lower portion of the trench;

forming a first insulation layer on the trench capacitor;

forming an epitaxy layer on the sidewalls of the trench above the first insulation layer as a liner to narrow the dimension of the trench; and

removing the first insulation layer uncovered by the epitaxy layer.

2. The method as claimed in claim 1, wherein the substrate is made of P-type silicon, N-type silicon, or non-doped epitaxy silicon.

3. The method as claimed in claim 1, wherein the first insulation layer is made of high density plasma oxide silicon.

4. The method as claimed in claim 1, wherein the epitaxy layer is made of P-type epitaxy silicon, N-type epitaxy silicon, or non-doped epitaxy silicon.

5. The method as claimed in claim 1, wherein the thickness of the epitaxy layer is 100~200 Å.

6. The method as claimed in claim 1, wherein the insulation layer uncovered by the epitaxy layer is removed by wet etching.

7. A method for increasing the capacitance of deep trench capacitors, comprising:

providing a substrate;

forming a pad structure on the substrate, wherein the pad structure comprises a pad oxide layer and a pad nitride silicon layer;

forming a patterned photoresist layer on the pad structure, wherein a trench region is defined by the region uncovered by the patterned photoresist layer, and the dimension of the region exceeds a predetermined dimension of the trench region;

etching the pad structure uncovered by the patterned photoresist layer using the patterned photoresist layer as a mask;

etching the substrate uncovered by the pad structure using the patterned photoresist layer and the pad structure as a mask, thereby forming a trench in the substrate;

removing the patterned photoresist layer;

forming a trench capacitor in the lower portion of the trench, wherein the trench capacitor comprises a buried electrode plate, a capacitor dielectric layer, and a first conductive layer, as another electrode plate of the trench capacitor;

forming a first insulation layer on the trench capacitor, the sidewalls of the trench, and the pad structure;

removing the first insulation layer covering the sidewalls of the trench and the pad structure by etching, thus forming the first insulation layer on the trench capacitor;

forming an epitaxy layer on the pad structure, the first insulation layer, and the sidewalls of the trench;

removing the epitaxy layer on the pad structure and the first insulation layer by etching, thus forming an epitaxy layer on the sidewalls of the trench as a liner to narrow the dimension of the trench; and

removing the first insulation layer uncovered by the epitaxy layer.

8. The method as claimed in claim 7, wherein the substrate is made of P-type silicon, N-type silicon, or non-doped epitaxy silicon.

9. The method as claimed in claim 7, wherein the pad oxide layer of the pad structure is formed by thermal oxidation.

10. The method as claimed in claim 7, wherein the pad nitride silicon layer of the pad structure is formed by chemical vapor deposition (CVD).

11. The method as claimed in claim 7, wherein the buried electrode plate of the trench capacitor is an N-type doped area.

12. The method as claimed in claim 7, wherein the capacitor dielectric layer of the trench capacitor is made of a stack layer comprising oxide-nitride (ON) or oxide-nitride-oxide (ONO) silicon.

13. The method as claimed in claim 7, wherein the first conductive layer of the trench capacitor is made of doped polycrystalline silicon or doped non-polycrystalline silicon.

14. The method as claimed in claim 7, wherein the first insulation layer is made of high density plasma oxide silicon.

15. The method as claimed in claim 7, wherein the epitaxy layer is made of P-type epitaxy silicon, N-type epitaxy silicon, or non-doped epitaxy silicon.

16. The method as claimed in claim 7, wherein the thickness of the epitaxy layer is 100~200 Å.

17. The method as claimed in claim 7, wherein the insulation layer uncovered by the epitaxy layer is removed by wet etching.